

INESC TEC | Research Grant (AE2025-00027)
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| Job Title | INESC TEC Research Grant (AE2025-00027) |
| Department | CTM |
| Institution | INESC TEC PORTO, , Portugal |
| Date Posted | Jan. 31, 2025 |
| Application Deadline | Feb. 12, 2025 |
| Position Start Date | Jan. 30, 2025 |
| Job Categories | Graduate Student |
| Academic Field(s) | Electrical and/or Electronics Computer Science Engineering - Other |
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| Apply By Email | |
| Job Description | |

Research Opportunities

Engineering

Work description

- Study the state of the art in mapping approaches for CGRA via AI methods and conventional methods.
- Familiarizing with existing methods in the working group for converting ONNX models to dataflow

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- graphs (DFGs), compiling via MLIR, and co-simulating RISC-V + CGRA.
- Determine the representations for the DFG and CGRA architectural specifications most suitable for use in machine learning methods.
 - Design and implement a machine learning-based method for mapping DFGs to the target CGRA architecture.
 - Generation of the configurations resulting from this mapping, and the programs for execution (via simulation) on the final RISC-V + CGRA system.
 - Collaboration in writing scientific articles to disseminate the results.

Academic Qualifications

- Master's degree in electrical engineering, computer science, or related field.

Minimum profile required

- Experience in hardware design or heterogeneous systems.
- Fluent in Portuguese and English (written and spoken).

Preference factors

- RISC-V and/or MLIR experience.
- Familiarity with ONNX and/or ML / AI frameworks.
- Fluent in English (written and spoken).

Application Period

Since 30 Jan 2025 to 12 Feb 2025

Centre

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Telecommunications and Multimedia

Scientific Advisor

[Nuno Miguel Paulino](#)

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Contact Information

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Contact

INESC TEC - Instituto De Engenharia De Sistemas E
Computadores, Tecnologia E Ciência

Portugal

Phone Number 222094000

Contact E-mail rh@inesctec.pt